3.3V CMOS Static RAM 1 Meg (64K x 16-Bit)

IDT71V016SA

Features

- 64K x 16 advanced high-speed CMOS Static RAM
- Equal access and cycle times
  - *— Commercial: 10/12/15/20ns*
  - *— Industrial: 12/15/20ns*
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly LVTTL-compatible
- Low power consumption via chip deselect
- Upper and Lower Byte Enable Pins
- Single 3.3V power supply
- Available in 44-pin Plastic SOJ, 44-pin TSOP, and 48-Ball Plastic FBGA packages

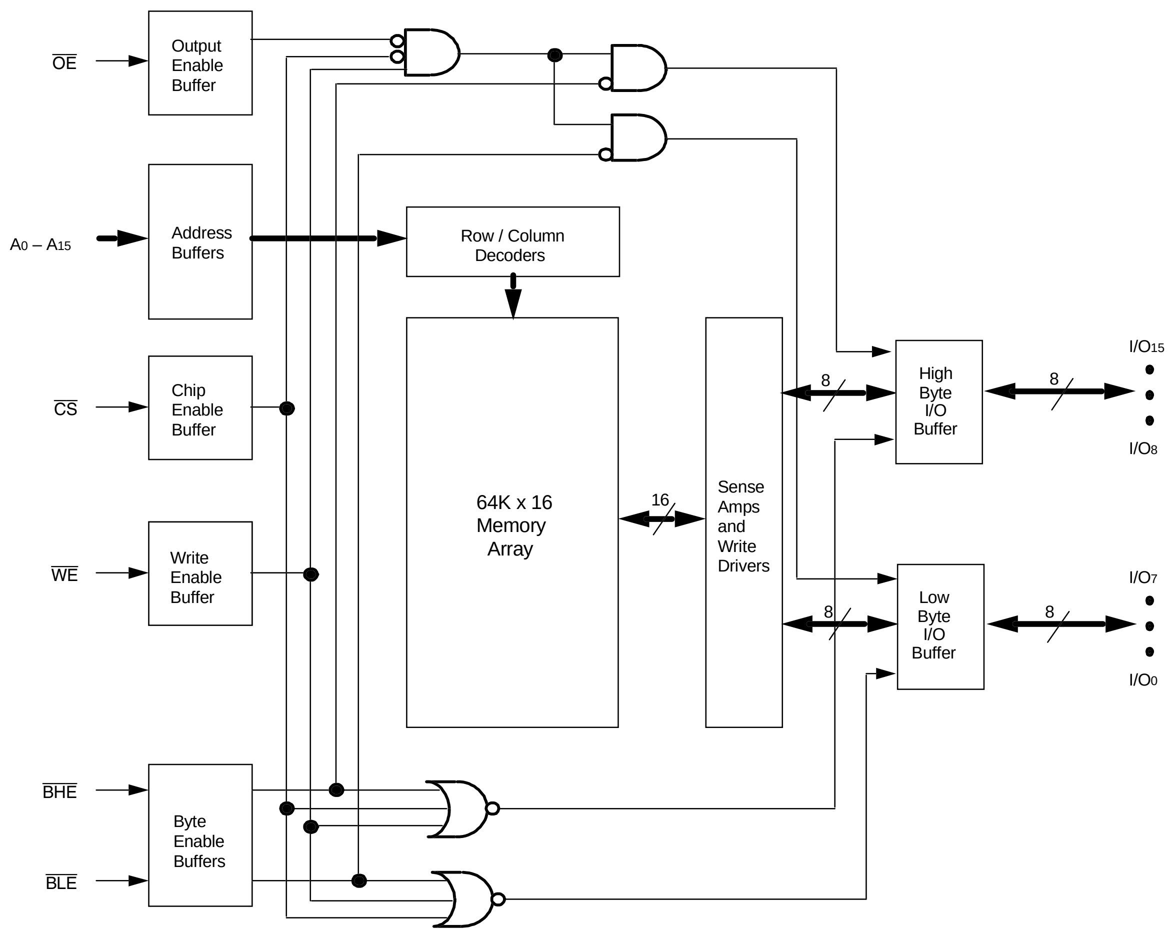
Description

The IDT71V016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V016 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V016 are LVTTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V016 is packaged in a JEDEC standard 44-pin Plastic SOJ, a 44-pin TSOP Type II, and a 48-ball plastic 7 x 7 mm FBGA.

Functional Block Diagram

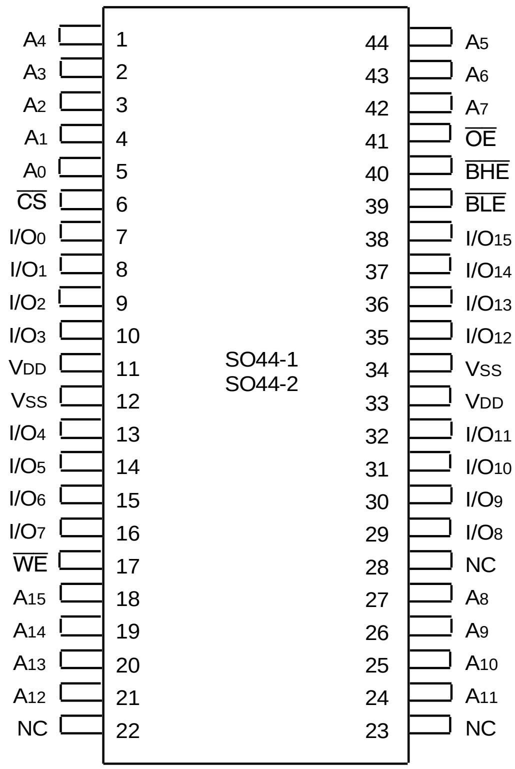


3834 drw 01

JUNE 2002

DSC-3834/06

Pin Configurations



3834 drw 02

SOJ/TSOP Top View

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CS}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{DD}
E	V_{DD}	I/O_{12}	NC	NC	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

3834 tbl 02a

FBGA (BF48-1) Top View

Pin Description

$A_0 – A_{15}$	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{BHE}$	High Byte Enable	Input
$\overline{BLE}$	Low Byte Enable	Input
$I/O_0 – I/O_{15}$	Data Input/Output	I/O
V_{DD}	3.3V Power	Power
V_{SS}	Ground	Gnd

3834 tbl 01

Truth Table[1]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0-I/O_7	I/O_8-I/O_{15}	Function
H	X	X	X	X	High-Z	High-Z	Deselected – Standby
L	L	H	L	H	$DATA_{OUT}$	High-Z	Low Byte Read
L	L	H	H	L	High-Z	$DATA_{OUT}$	High Byte Read
L	L	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Word Read
L	X	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Word Write
L	X	L	L	H	$DATA_{IN}$	High-Z	Low Byte Write
L	X	L	H	L	High-Z	$DATA_{IN}$	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

3834 tbl 02

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't care.

Absolute Maximum Ratings[1]

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage Relative to V_{SS}	–0.5 to +4.6	V
V_{IN}, V_{OUT}	Terminal Voltage Relative to V_{SS}	–0.5 to V_{DD}+0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

3834 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

3834 tbl 06

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	Vss	VDD
Commercial	0°C to +70°C	0V	See Below
Industrial	-40°C to +85°C	0V	See Below

3834 tbl 04

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}[1]	Supply Voltage	3.15	3.3	3.6	V
V_{DD}[2]	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3[3]	V
V_{IL}	Input Low Voltage	–0.3[4]	—	0.8	V

3834 tbl 05

NOTES:
1. For 71V016SA10 only.
2. For all speed grades except 71V016SA10.
3. V_{IH} (max.) = V_{DD}+2V for pulse width less than 5ns, once per cycle.
4. V_{IL} (min.) = –2V for pulse width less than 5ns, once per cycle.

DC Electrical Characteristics

(V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71V016SA Min.	IDT71V016SA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = V_{SS} to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{DD}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{DD} = Min.	2.4	—	V

3834 tbl 07

DC Electrical Characteristics[1,2]

(V_{DD} = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} – 0.2V)

Symbol	Parameter		71V016SA10 Com'l Only	71V016SA12 Com'l	71V016SA12 Ind	71V016SA15 Com'l	71V016SA15 Ind	71V016SA20 Com'l	71V016SA20 Ind	Unit
I_{CC}	Dynamic Operating Current $\overline{CS}$ ≤ V_{LC}, Outputs Open, V_{DD} = Max., f = f_{MAX}[3]	Max.	160	150	160	130	130	120	120	mA
		Typ.[4]	125	120	--	110	--	110	--	
I_{SB}	Dynamic Standby Power Supply Current $\overline{CS}$ ≥ V_{HC}, Outputs Open, V_{DD} = Max., f = f_{MAX}[3]		45	40	45	35	35	30	30	mA
I_{SB1}	Full Standby Power Supply Current (static) $\overline{CS}$ ≥ V_{HC}, Outputs Open, V_{DD} = Max., f = 0[3]		10	10	10	10	10	10	10	mA

3834 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V_{DD} – 0.2V (High).
3. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing .
4. Typical values are measured at 3.3V, 25°C and with equal read and write cycles.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

3834 tbl 09

AC Test Loads

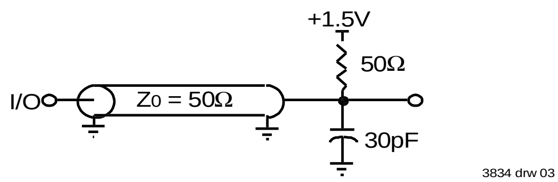
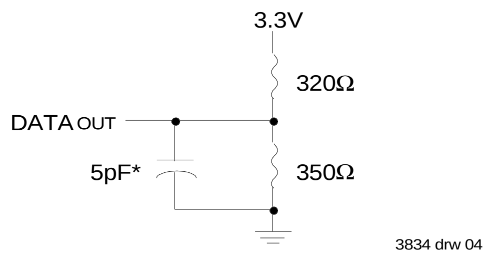


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

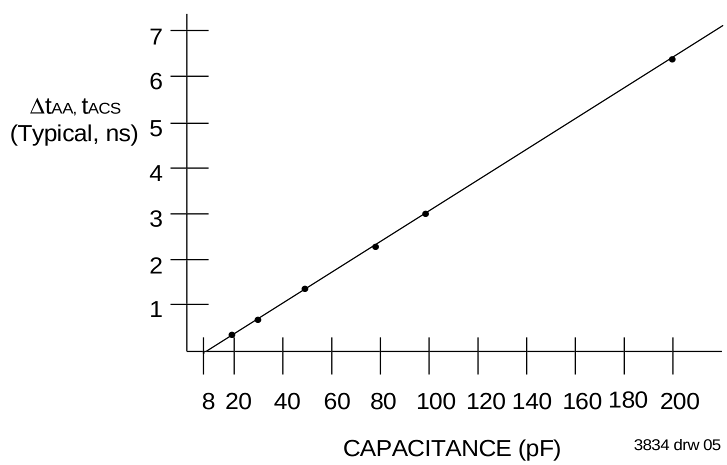


Figure 3. Output Capacitive Derating

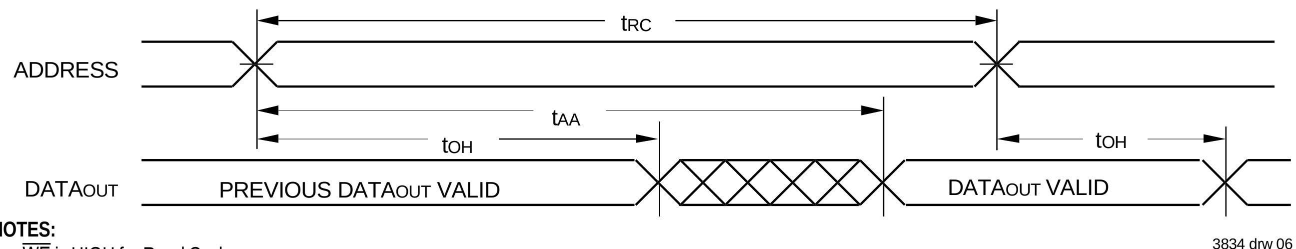
AC Electrical Characteristics (VDD = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	71V016SA10(2)		71V016SA12		71V016SA15		71V016SA20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
t_{CLZ}(1)	Chip Select Low to Output in Low-Z	4	—	4	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Select High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t_{OE}	Output Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t_{OLZ}(1)	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t_{BE}	Byte Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t_{BLZ}(1)	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{BHZ}(1)	Byte Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	7	—	8	—	10	—	12	—	ns
t_{CW}	Chip Select Low to End of Write	7	—	8	—	10	—	12	—	ns
t_{BW}	Byte Enable Low to End of Write	7	—	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	10	—	12	—	ns
t_{DW}	Data Valid to End of Write	5	—	6	—	7	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}(1)	Write Enable High to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable Low to Output in High-Z	—	5	—	6	—	6	—	8	ns

3834 tbl 10

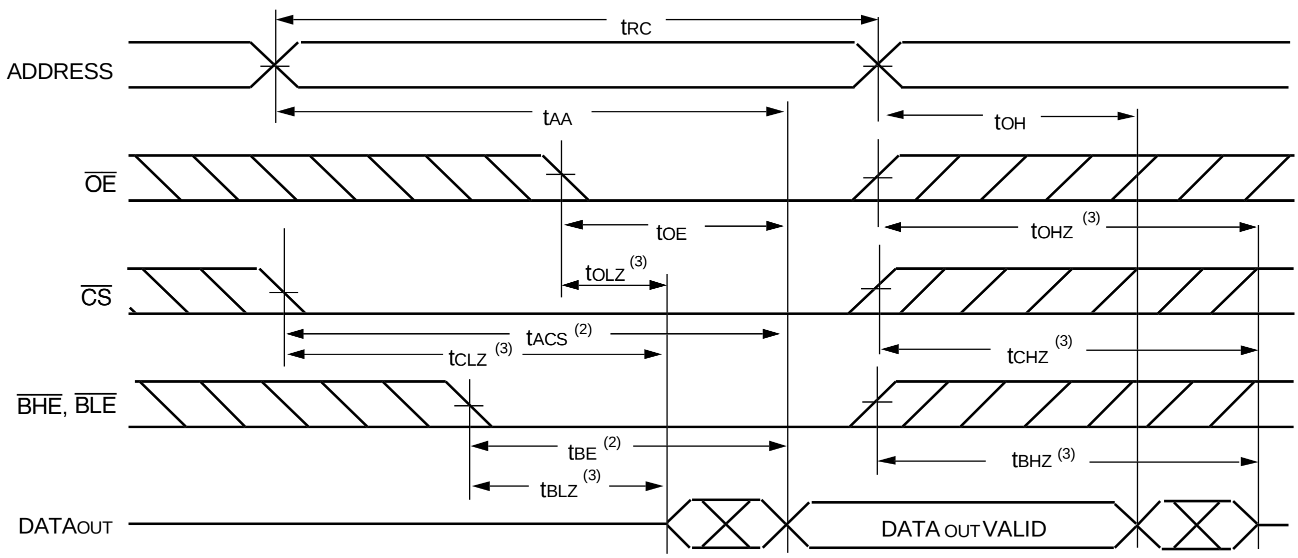
NOTES:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. 0°C to +70°C temperature range only.

Timing Waveform of Read Cycle No. 1(1,2,3)



NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.

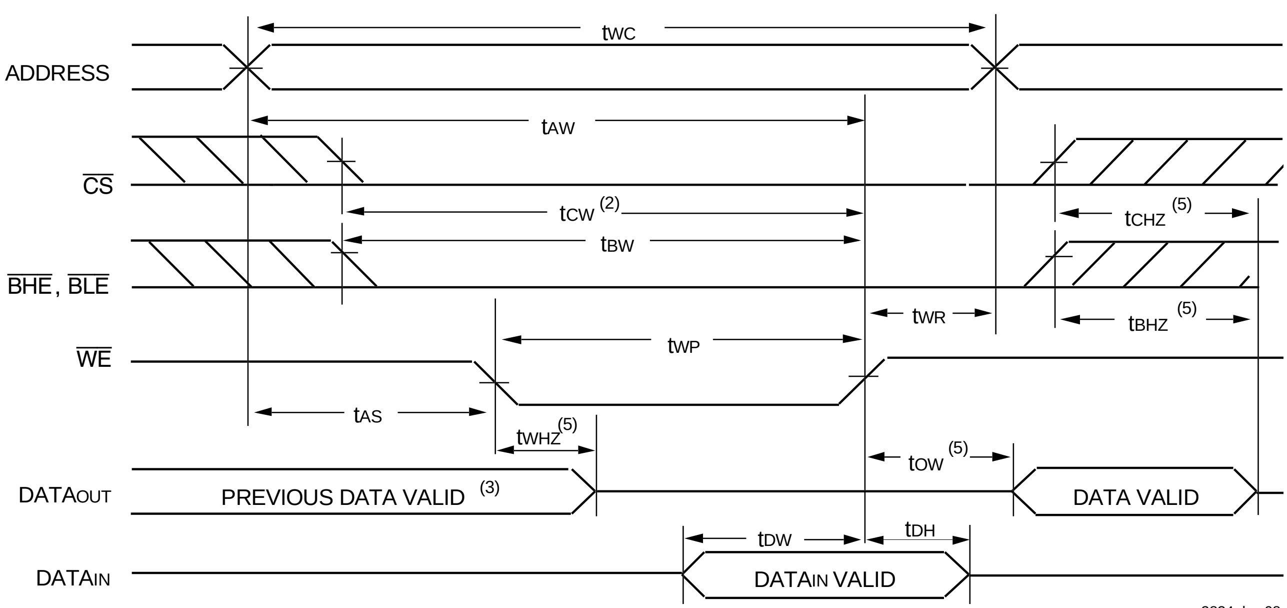
Timing Waveform of Read Cycle No. 2[1]



3834 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured ±200mV from steady state.

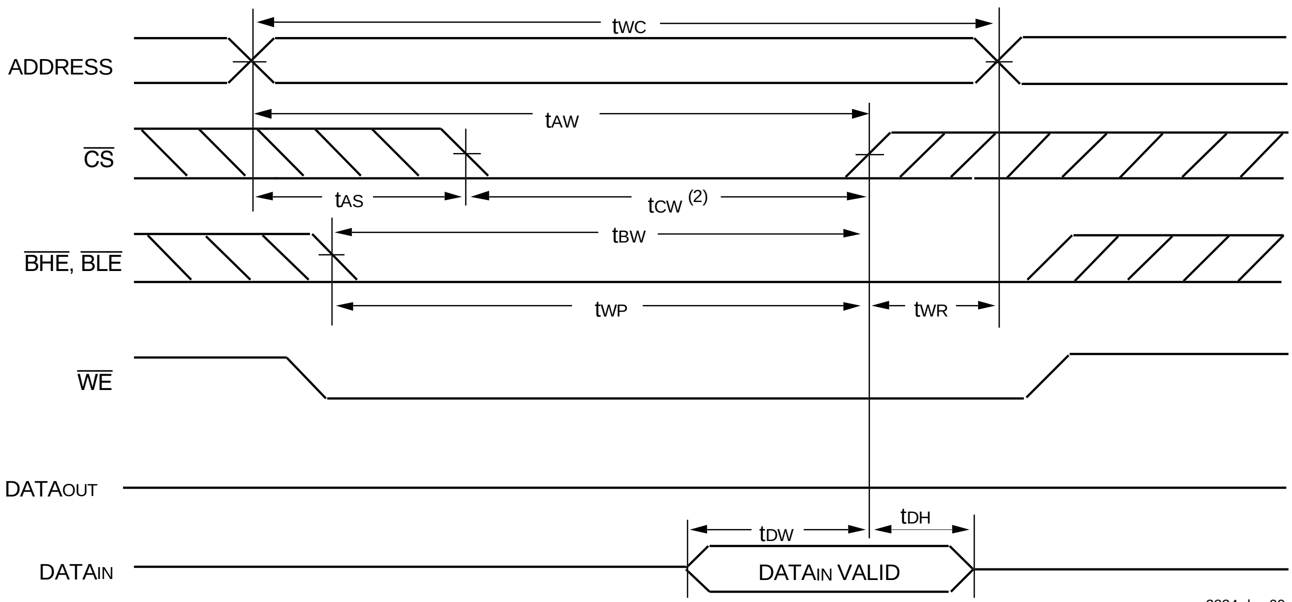
Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)[1,2,4]



3834 drw 08

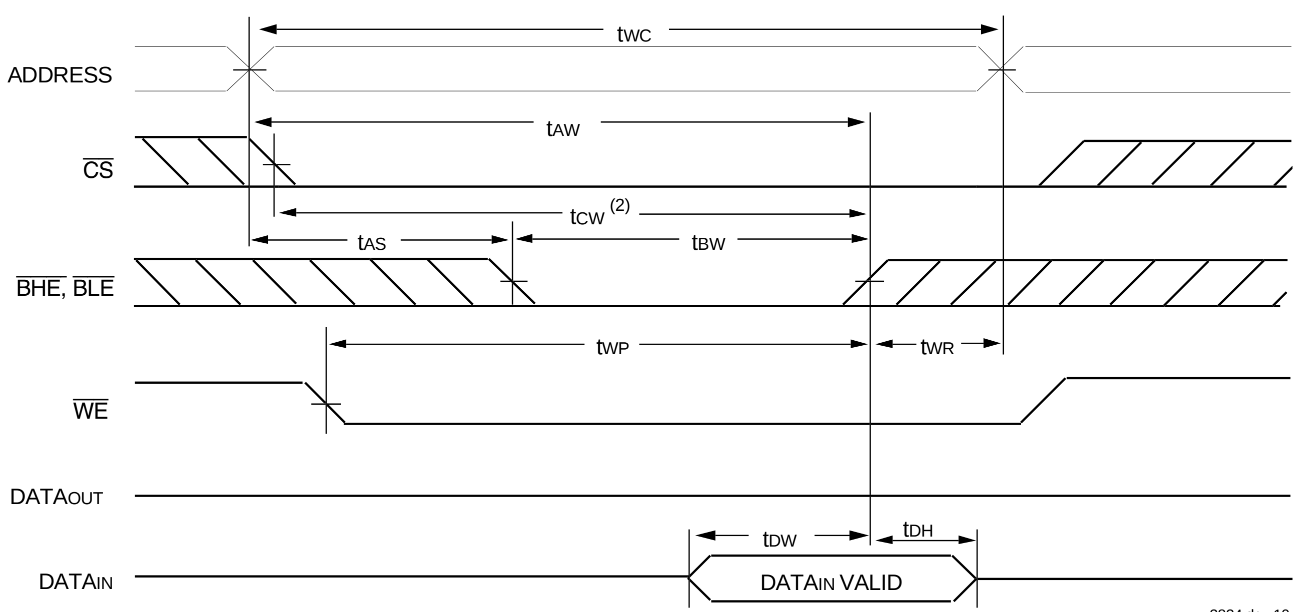
NOTES:
1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,4)



3834 drw 09

Timing Waveform of Write Cycle No. 3 ($\overline{BHE}$, $\overline{BLE}$ Controlled Timing)(1,4)



3834 drw 10

NOTES:
1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Ordering Information

IDT 71V016 SA XX XXX X X

Device Type | Power | Speed | Package | Process/Temperature Range | Tape & Reel

Tape & Reel:
- 8

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- I — Industrial (-40°C to +85°C)

Package:
- Y — 400-mil SOJ (SO44-1)
- PH — 400-mil TSOP Type II (SO44-2)
- BF — 7.0 x 7.0 mm FBGA (BF48-1)

Speed:
- 10**
- 12
- 15
- 20

Speed in nanoseconds

** Commercial temperature range only.

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Datasheet Document History

1/7/00		Updated to new format
	Pp. 1, 3, 5, 8	Added Industrial Temperature range offerings
	Pg. 2	Numbered I/Os and address pins on FBGA Top View
	Pg. 6	Revised footnotes on Write Cycle No. 1 diagram
	Pg. 7	Revised footnotes on Write Cycle No. 2 and No. 3 diagrams
	Pg. 9	Added Datasheet Document History
08/30/00	Pg. 3	Tighten I_{CC} and I_{SB}.
	Pg. 5	Tighten t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ} and t_{WHZ}
08/22/01	Pg. 8	Removed footnote "available in 15ns and 20ns only"
06/20/02	Pg. 8	Added tape and reel field to ordering information

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